SA58646

UHF 900 MHz transceiver IC

Rev. 01.05 — 14 July 2006 Objective data sheet

1. General description

The SA58646 is a BiCMOS integrated circuit that performs all functions from the antenna to the microcontroller for reception and transmission for both the base station and the handset in a 902 MHz to 928 MHz full-duplex radio. The SA58646 may be used in a UHF push-to-talk walkie-talkie or in a UHF to 900 MHz data transceiver. The SA58646 is a pin compatible derivative of the UAA3515 with advanced features.

This IC integrates most of the functions required for a half-duplex or full-duplex radio in a single integrated circuit. Additionally, the programmability implemented reduces significantly external components count, board space requirements and external adjustments.

2. Features

2.1 RF RX (single frequency conversion FM receiver)

- Integrated LNA
- Image reject mixer
- FM detector at 10.7 MHz including an IF limiter, a wide band PLL demodulator, an output amplifier and a RSSI output
- carrier detect with programmable threshold
- programmable data amplifier (slicer) phase

2.2 RF TX

- Buffer driving an internal PA with programmable gain
- Data transmission summator operational amplifier

2.3 Synthesizer

- Crystal reference oscillator with integrated tuning capacitor
- Reference frequency divider
- Narrow band Rx PLL including Rx VCO with integrated varicaps
- Narrow band Tx PLL including Tx VCO with integrated varicaps
- VCOs external inductors can be done with printed transmission line on PCB which offer substantial savings
- Programmable clock divider with output buffer to drive a microcontroller

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2.4 Baseband RX section

- Programmable RX gain (enable volume control phone feature)
- Expander with output noise level control
- Earpiece amplifier with volume control feature
- Data amplifier

2.5 Baseband TX section

- Microphone amplifier
- Compressor with Automatic Level Control and Hard Limiter
- Programmable TX gain

2.6 Microcontroller interface

- 3-wire serial interface

2.7 Other features

- Voltage regulator to supply internal PLLs
- Selectable voltage doubler
- Programmable low battery detect time multiplexed with RSSI carrier detect

3. Applications

- 902 MHz to 928 MHz full-duplex radio
- UHF to 900 MHz data transceiver
- UHF push-to-talk walkie-talkie

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SA58646BD	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-1

5. Block diagram

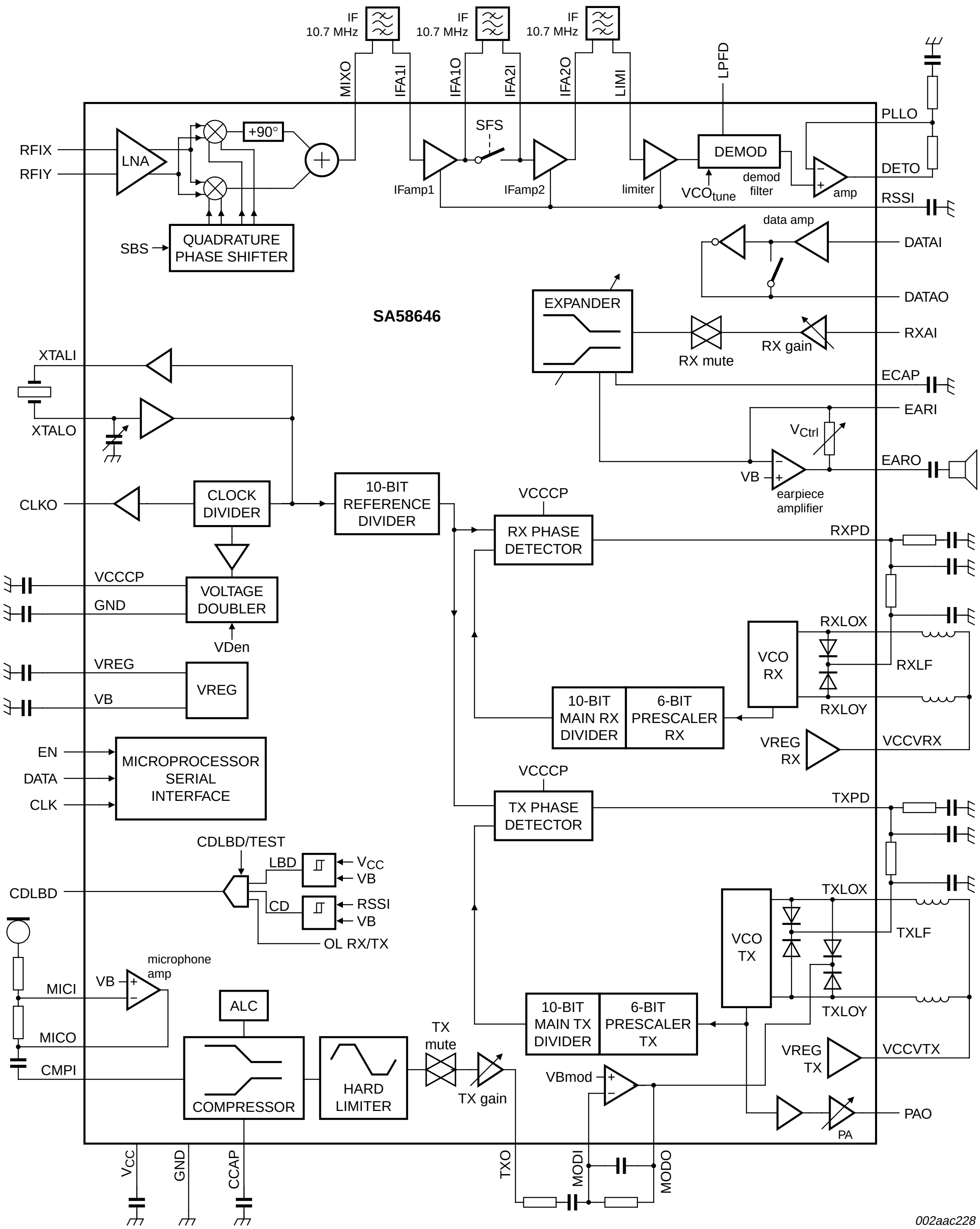


Fig 1. Block diagram of SA58646

6. Pinning information

6.1 Pinning

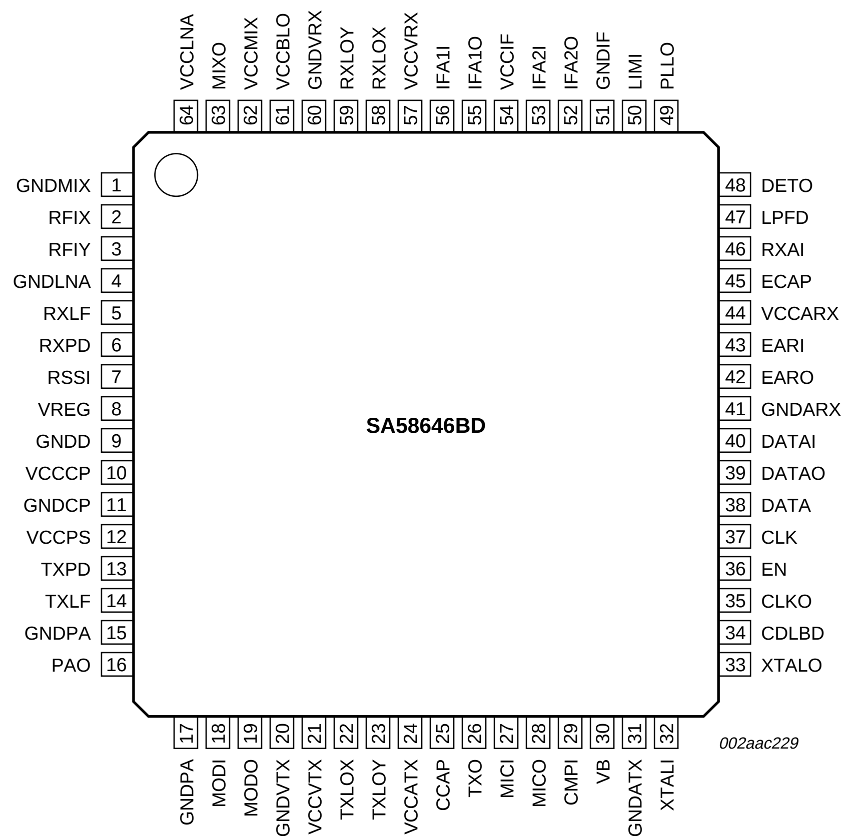


Fig 2. Pin configuration for LQFP64

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
GNDMIX	1	mixers negative supply
RFIX	2	LNA input
RFIY	3	LNA input
GNDLNA	4	LNA negative supply
RXLF	5	RX loop filter output
RXPD	6	RX phase detector output
RSSI	7	RSSI output
VREG	8	pin for internal regulator
GNDD	9	digital negative voltage supply
VCCCP	10	voltage doubler or external positive supply for charge pumps
GNDCP	11	charge pump negative voltage supply

Table 2. Pin description *…continued*

Symbol	Pin	Description
VCCPS	12	prescaler positive supply
TXPD	13	TX phase detector output
TXLF	14	TX loop filter output
GNDPA	15	PA negative supply
PAO	16	PA output
GNDPA	17	PA negative supply
MODI	18	summator amplifier input
MODO	19	summator amplifier output
GNDVTX	20	VCO TX negative voltage supply
VCCVTX	21	VCO TX positive voltage supply
TXLOX	22	VCO TX pin
TXLOY	23	VCO TX pin
VCCATX	24	TX audio positive voltage supply
CCAP	25	external capacitor for compressor
TXO	26	audio TX output
MICI	27	microphone amplifier input
MICO	28	microphone amplifier output
CMPI	29	compressor input
VB	30	voltage reference
GNDATX	31	TX audio negative supply
XTALI	32	XTAL input
XTALO	33	XTAL output
CDLBD	34	carrier detect or low battery detect output (out of lock synthesizer RX and/or TX in Test mode)
CLKO	35	clock output
EN	36	enable signal for serial interface
CLK	37	clock signal for serial interface
DATA	38	data signal for serial interface
DATAO	39	data amplifier output
DATAI	40	data amplifier input
GNDARX	41	audio RX negative supply
EARO	42	earpiece amplifier output
EARI	43	earpiece amplifier input
VCCARX	44	audio RX positive supply
ECAP	45	external capacitor for expander
RXAI	46	audio RX input
LPFD	47	demodulator loop filter
DETO	48	inverting demodulator amplifier output
PLLO	49	demodulator amplifier negative input
LIMI	50	limiter input
GNDIF	51	IF negative supply

Table 2. Pin description *…continued*

Symbol	Pin	Description
IFA2O	52	IF second amplifier output
IFA2I	53	IF second amplifier input
VCCIF	54	IF positive supply
IFA1O	55	IF first amplifier output
IFA1I	56	IF first amplifier input
VCCVRX	57	VCO RX positive voltage supply
RXLOX	58	VCO RX pin
RXLOY	59	VCO RX pin
GNDVRX	60	VCO RX negative voltage supply
VCCBLO	61	RX LO buffer positive supply
VCCMIX	62	mixers positive supply
MIXO	63	mixer output
VCCLNA	64	LNA positive supply

7. Functional description

Refer to Figure 1 "Block diagram of SA58646".

7.1 Power supply and power management

7.1.1 Power supply voltage

This circuit is used in a full-duplex radio handset and base unit. The handset unit is battery powered and can operate on three NiCad cells. The minimum supply voltage of the IC is V_{CC} = 2.9 V.

7.1.2 Power saving operation modes

When the circuit is used in a handset, it is important to reduce current consumption. There are 3 main modes of operation. In Active (talk) mode all blocks are powered. In RX mode, all circuitry in the RF receiver part is active. In Inactive mode, all circuitry is powered down except the serial interface. In this latter mode Xtal reference oscillator, output clock buffer, voltage regulator and voltage doubler can be separately disabled. A low current consumption mode on the Xtal oscillator and clock output can be programmed. Latch memory is maintained in all modes. Table 3 shows which blocks are powered in each mode.

Table 3. Powered blocks

Circuit block	Active mode	RX mode	Inactive mode
VB reference	X	X	-
RF receiver	X	X	-
RX PLL	X	X	-
Rx and Tx audio	X	-	-
RF Tx (and PA if enable)	X	-	-

Some blocks can be activated separately: crystal oscillator, voltage regulator (adjustment is always disabled), power amplifier, voltage doubler, hard limiter, ALC, output clock buffer and earpiece amplifier. The following table shows which block can be activated in each mode.

Table 4. Activated blocks

Circuit block	Active mode	RX mode	Inactive mode
XTAL active[1]	X	X	X
Clock out not disabled	X	X	X
Vreg active[2]	X	X	X
PA active (PA2 = 1)	X	-	-
Doubler enabled[3]	X	X	X
Hard limiter or ALC not disabled	X	-	-
Earpiece amplifier (earpiece enable = 1)	X	X	-[4]

[1] In RX and TX mode, XTAL is automatically activated. An external frequency can be forced to the crystal pins.

[2] In RX and TX mode, the voltage regulator with adjustment is automatically enabled whatever Vreg bit is activated or not.

[3] If voltage doubler is enabled, the XTAL is automatically activated.

[4] In Inactive mode, the earpiece amplifier is automatically disabled.

7.1.3 Control bits in power saving modes

Table 5 shows the control bit values for selection of each mode and the typical current consumption for those modes.

Table 5. Control bit values

Active mode, bit 1	Active mode, bit 0	Power saving mode	Typical current consumption (V_{CC} = 3.3 V; T_{amb} = 25 °C; XTAL = 10.24 MHz
1	1	Active mode	76 mA
1	0	RX mode	58 mA
0	X	Inactive mode	<10 μA (with voltage doubler inactive, Xtal disabled, VREG disabled, CLKO disabled)
			210 μA (with voltage doubler inactive, Xtal HIGH = 0, VREG disabled, CLKO disabled)
			300 μA (with voltage doubler inactive, Xtal HIGH = 1, VREG disabled, CLKO disabled)
			550 μA (with voltage doubler inactive, Xtal HIGH = 1, VREG enabled, CLKO disabled)
			690 μA (with voltage doubler enabled, Xtal HIGH = 1, VREG enabled, CLKO disabled)

When clock out is activated, an extra power consumption is applied which is proportional to the programmed CLKO Drive bit. In XTAL HIGH = 0 mode, the crystal loss is less than 50 Ω to ensure reliable start-up.

Table 6. Extra power consumption

Divider ratio	Extra consumption	
	CLKO Drive = 0	CLKO Drive = 1
1, 2, 2.5, 4, 128	520 μA	350 μA
off	0 μA	0 μA

7.2 The FM receiver part (RXRF)

The FM receiver has a single frequency conversion architecture. The image reject mixer enables the user to save an RF filter. The Side Band Select feature enables the user to choose its frequency plan with RxLO in or out of ISM band and have the same IC for both base and handset. IF channel filtering compromise between price and performance can be achieved using two or three 10.7 MHz external filters. The integrated FM-PLL demodulator with limiter enables consistent saving on external components and pins.

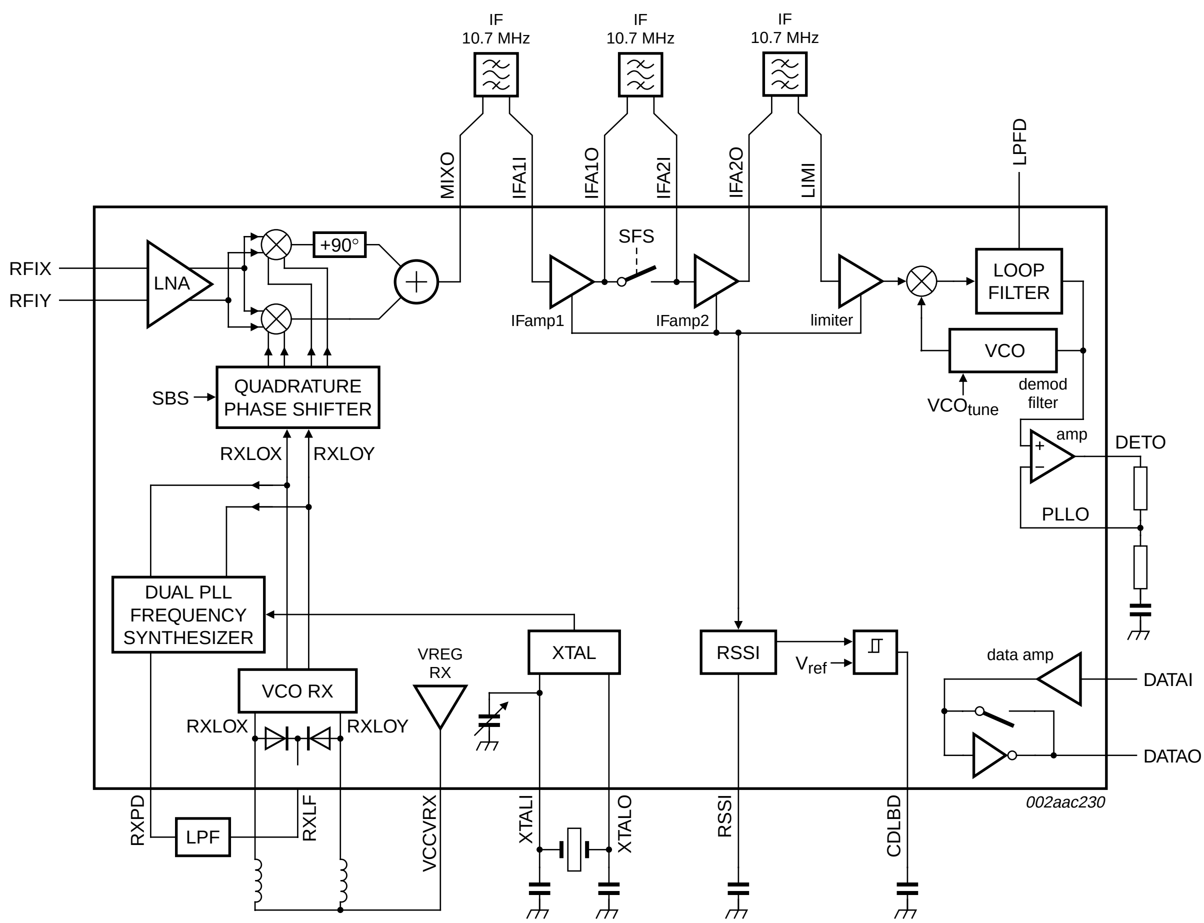


Fig 3. FM receiver block diagram

7.2.1 Data comparator

The data comparator is an inverting hysteresis comparator. The open collector output is current limited to control the output signal slew rate. An external band pass filter is connected between DETO and DATAI (AC coupled). External resistor should be 180 kΩ with V_{CC} maximum. An external capacitor can be added to further reduce the slew rate.

7.3 The transmit part

The transmitter architecture is of the direct modulation type. The transmit VCO will be frequency modulated by either speech or data (see Figure 4).

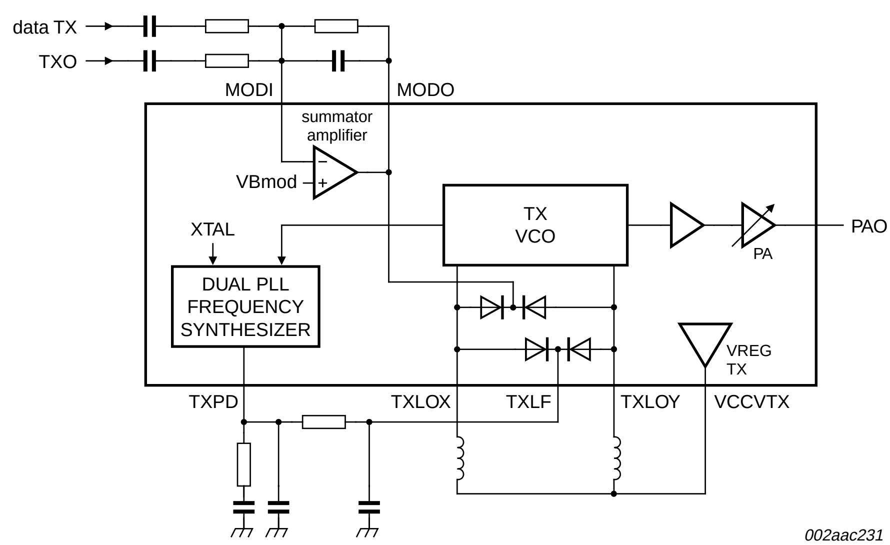


Fig 4. Transmit block diagram

7.3.1 Transmit VCO

Before the VCO, an amplifier sums the modulating signal and the data TX signal. VCO varicaps are integrated. External inductors that are in series with bonding wires and lead frame are needed to obtain the right frequency. The power amplifier is capable of driving 50 Ω. The output level is programmed with 2 bits through the serial bus interface.

7.4 The synthesizer

The crystal local oscillator and reference divider provide the reference frequency for the RX and TX PLLs. The 10-bit programmed divider value for the reference divider is selected based on the crystal frequency, the desired RX and TX reference frequency values. The crystal frequency of 16.348 MHz is chosen to provide to the microcontroller the standard 4.096 MHz frequency when programming the clock divider value to 4. Then 16.384 MHz crystal frequency is proposed. The clock divider value will be programmed to 1, 2, 2.5, 4 and 128. The clock divider value of 128 is chosen to place the IC in Sleep mode which enables current saving in the microcontroller. Clock output is an emitter follower type.

The 16-bit TX counter is programmed for the desired transmit channel frequency. The 16-bit RX counter is programmed for the desired local oscillator frequency. Counters are built with a 6-bit prescaler (divider value R from 64 to 127) and a 10-bit CMOS divider (divider value C from 8 to 1023). The full counter then provides a divider value from 512 to 65535. To calculate the settings of the two counters, the following procedure is used:

$C = \text{int}\,(M/64)$

$R = M - C \times 64$

with M being the division ratio between the VCO frequency and the reference frequency.

Example: RF Rx = 903 MHz, VCO Rx = 892.3 MHz, IF = 10.7 MHz,
VCO Tx = 925.6 MHz and the internal comparison frequency 20 kHz (Xtal = 10.24 MHz):
RefDiv = 512 (10 0000 0000), M Rx = 892.3e6/20e3 = 44615,
C Rx = 697 (10 1011 1001), R Rx = 7 (00 0111) and M Tx = 925.6e6/20e3 = 46280,
C Tx = 723 (10 1101 0011), R Tx = 8 (00 1000).

VCOs and varicaps are integrated. The total equivalent inductance is comprised of the bonding wires, lead frame of the package and external inductors. External inductors can be directly done with a printed transmission line on PCB, which allow substantial savings.

An on-chip selectable voltage doubler is provided to enable a larger tuning range of the VCOs. The phase detectors have current drive type outputs. Current can be chosen between 400 μA and 800 μA.

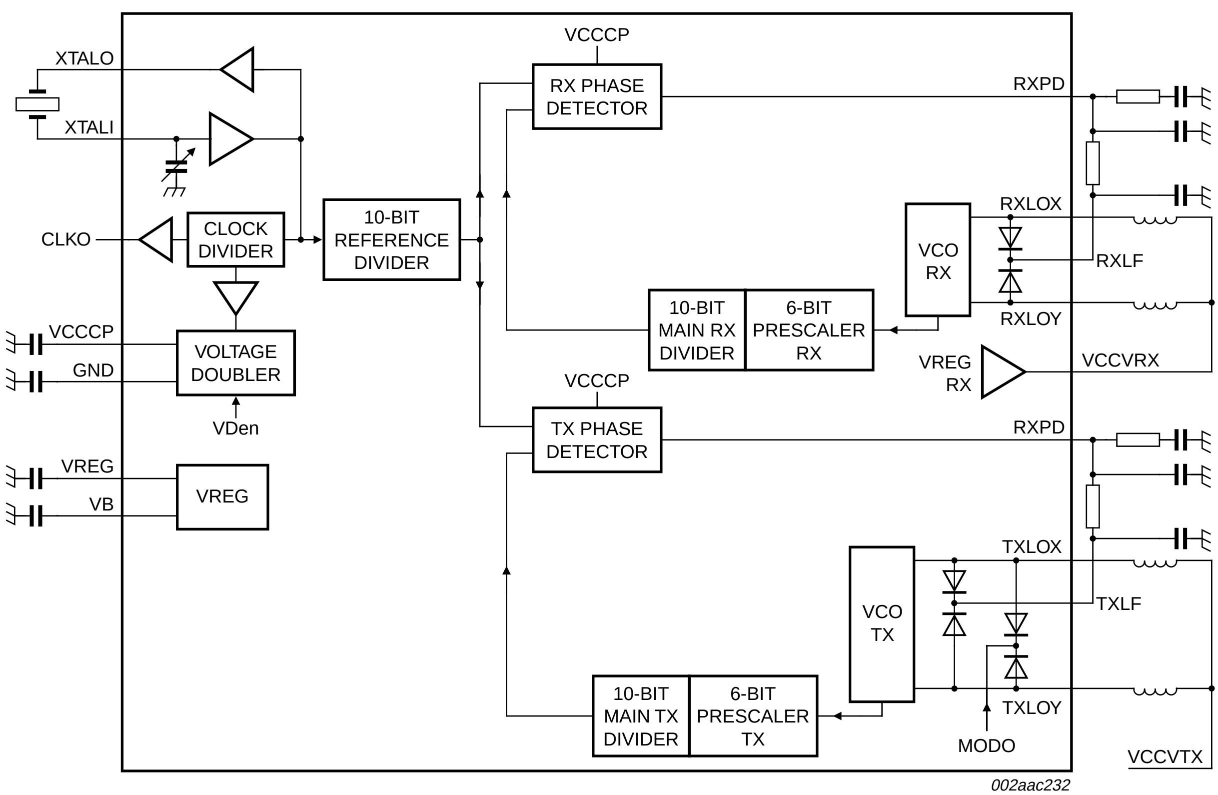


Fig 5. Synthesizer block diagram

7.5 The RX baseband

This section covers the RX Audio path from pins RXAI to EARO. The RXAI input signal is AC-coupled.

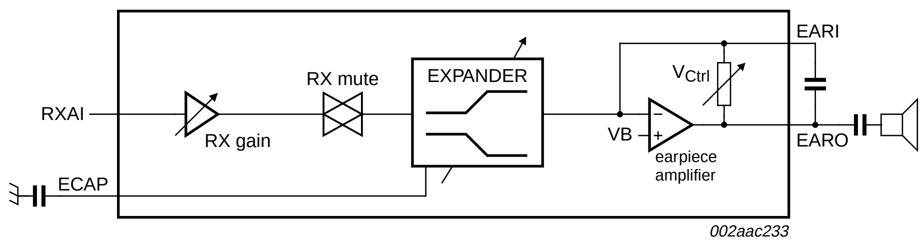


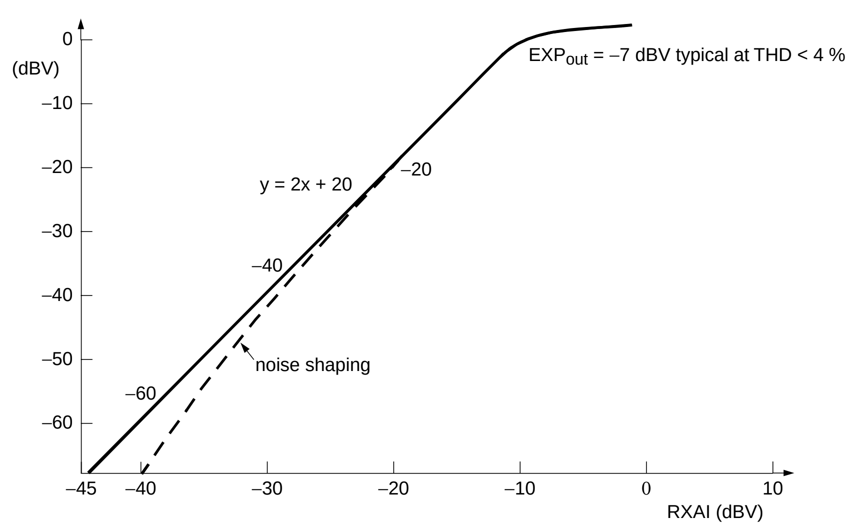
Fig 6. RX baseband block diagram

The microcontroller sets the value of the RX Gain with 32 linear steps of 0.5 dB. The RX baseband has a mute and an expander with the characteristics shown in Figure 7.

The audio level is programmable over a dynamic range of 31 dB by the Rx_Gain control. The expander slope multiplies the RX Gain step by 2 to achieve 1 dB steps on the earpiece output.

Noise coming from and in the RX baseband can be shaped thanks to a ‘noise control’ programmability. It provides the possibility to attenuate the expander gain at low input level. Figure 7 provides some information about the noise shaper function.

The earpiece amplifier is an inverting rail-to-rail operational amplifier. The non-inverting input is connected to the internal VB reference. Software volume control on the earpiece amplifier is done by integrated switched feedback resistances. Volume control tuning range is 14 dB. Hardware volume control is done by externally switching the earpiece feedback resistance.



RX gain adjust = 0 dB; VCtrl = 0 dB; no external resistance

Fig 7. Expander characteristic

7.6 The TX baseband

This section covers the TX audio path from pins MICI to TXO. The input signal at pin MICI is AC-coupled. The microphone amplifier output is also AC-coupled.

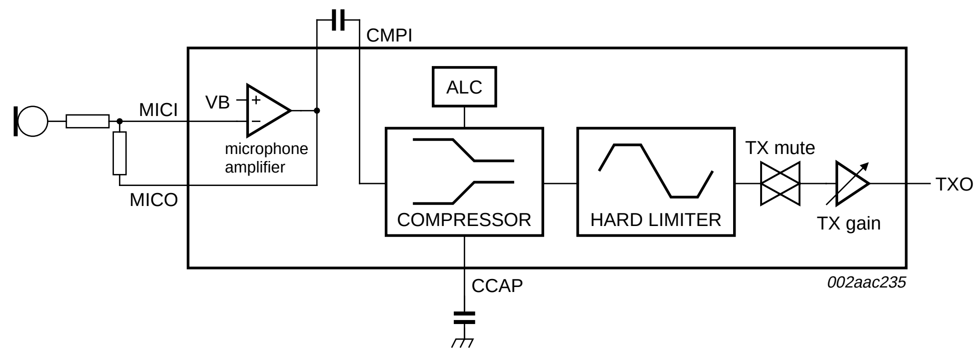


Fig 8. TX baseband block diagram

The microphone amplifier is an inverting operational amplifier whose gain can be set by external resistors. The non-inverting input is connected to the internal VB reference. External resistors are used to set the gain and frequency response.

The TX baseband has a compressor with the characteristic shown in Figure 9. The ALC (Automatic Level Control) provides a 'soft' limit to the output signal swing as the input voltage increases slowly (that is, a sine wave is maintained at the output). A hard limiter clamps the compressor output voltage at $1.26V_{(p\text{-}p)}$. The ALC and hard limiter can be disabled through the microcontroller interface. The hard limiter is followed by a mute. The TX Gain is digitally programmable with 32 steps of 0.5 dB.

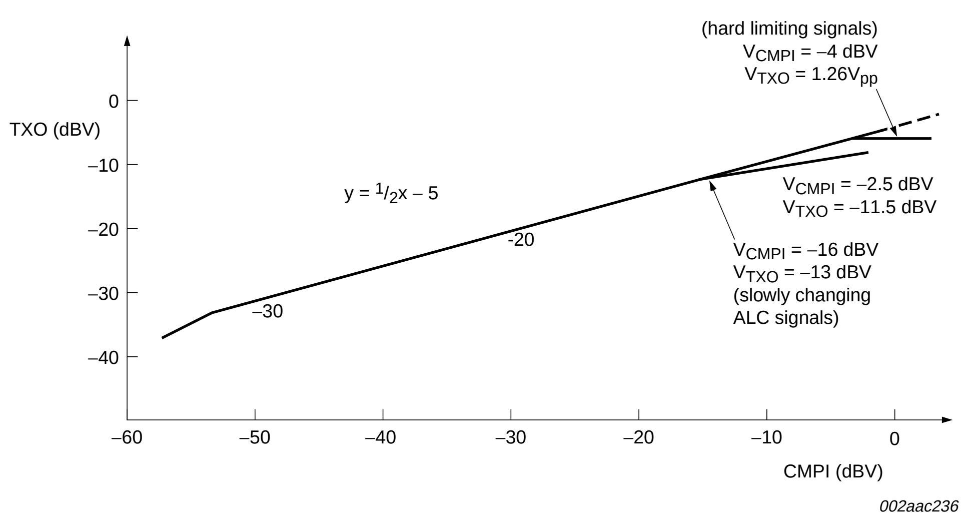


Fig 9. Compressor characteristic

7.7 Other features

7.7.1 Voltage regulator

The VREG pin is the internal supply voltage for the RX and TX PLLs. It is regulated at 2.7 V nominal voltage. The V_{CC} pin is the supply voltage input for the internal voltage regulator. Two capacitors with 4.7 μF and 100 nF values must be connected to the VREG pin to filter and stabilize this regulated voltage. The tolerance of the regulated voltage is initially ± 8 % but is improved to ± 2 % after the internal band gap voltage reference is adjusted through the microcontroller. In the Inactive mode, the regulator voltage adjustment is automatically disabled.

7.7.2 Low battery detect

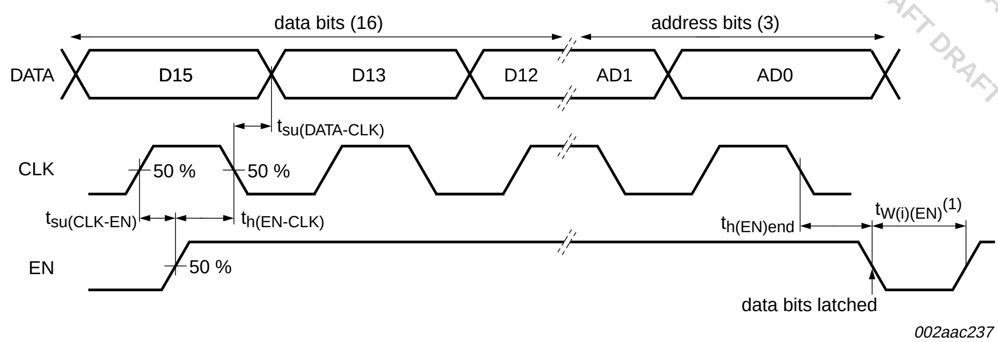
The low battery detect measures the voltage level of the V_{CC} with a resistor divider and a comparator. One input of the comparator is connected to VB; the other is connected to the middle point of the resistor divider. To prevent spurious switching the comparator has a built-in hysteresis. The precision of the detection depends on the divider accuracy, the comparator offset and the accuracy of the reference voltage. The output is multiplexed at the CDLBD pin. When the battery voltage level is under the threshold voltage, the CDLBD output is set at logic LOW.

7.8 Microcontroller serial interface

The serial interface is used for programming of the IC. 19 bits (16 bits for data and 3 bits for registers) are used to program the IC. The serial interface requires 3 pins: DATA, CLK, EN. The serial interface pins are supplied by VREG. The ESD protection diodes on these pins are connected to V_{CC}. Digital outputs (CDLBD, DATAO) have open collector or open-drain; CLKO is an emitter-follower output.

The DATA, CLK and EN pins provide a 3-wire unidirectional serial interface for programming the reference counters, the transmit and receive channel divider counters, and the control functions.

The interface consists of 19-bit shift registers connected to a matrix of registers organized as 7 words of 16 bits (all control registers). The data is entered with the most significant bit first. The leading 16 bits include the data (D15 to D0), while the trailing 3 bits setup the address (AD2 to AD0). The first bit entered is D15, the last bit AD0. The DATA and CLK pins are used to load data into the shift register. Figure 11 shows the timing required on all pins. Data is clocked into the shift registers on negative clock transitions.



(1) The minimum pulse width should be equal to the period of the comparison frequency. The synthesizer checks the internal EN signal not to happen during a comparison phase to avoid any phase error jump. Then this time can be reduced to 100 ns for words which do not influence the synthesizer (word 1, 2, 3).

Fig 10. Digital signals timing requirement (except clock divider programming)

A new clock divider ratio is enabled thanks to an extra EN rising edge. Minimum hold time is 50 ns. During that time, no clock cycle is allowed. These extra EN edges can be applied to all the data programmed, but will have no effect on the serial interface programming.

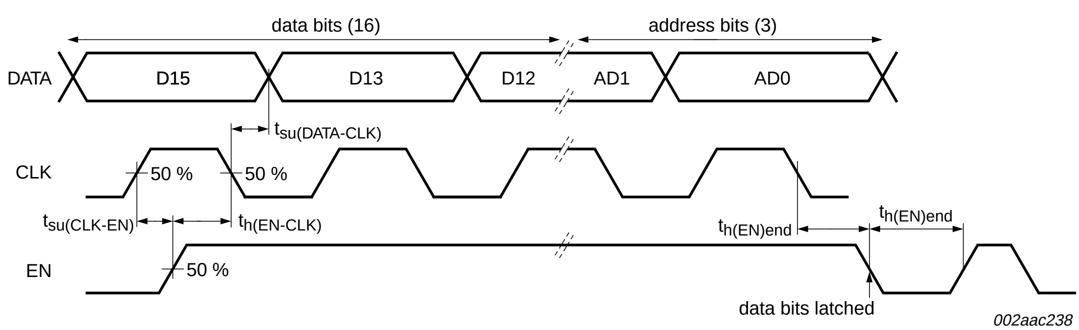


Fig 11. Digital signals timing requirement for clock divider programming

7.8.1 Data registers and addresses

D15 is the most significant bit, and is written first. Table 7 shows the data latches and addresses which are used to select each of the registers.

Table 7. Data registers

Addr	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
000	SBS	volume control [1:0]		earpiece enable	RX gain [4:0]					SFS	DATA Phase	FM-PLL VCO tuning [4:0]				
001	RX prescaler [5:0]						RX main divider [9:0]									
010	[1]						reference divider [9:0]									
011	TX prescaler [5:0]						TX main divider [9:0]									
100	Test mode 2	CLKO drive	Test mode 1	doubler enable	TX gain [4:0]					TX mute	hard limiter enable	ALC disable	Xtal active	RX mute	Demod filter	[1]
101	VREG enable	Mode [1:0]		Xtal HIGH	carrier detect levels [4:0]					low battery detect levels [2:0]			battery detect active	clock divider [2:0]		
110	PA output [2:0]			TX charge pump current	RX charge pump current	voltage reference adjust [2:0]			noise expander control [1:0]		Test mode 0	[1]	Xtal tuning cap [3:0]			

[1] Undefined zone should always be programmed with 0.

Table 8. Preset values at power-on

Addr	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
000	0	11		0	01111					1	0	01111				
001	XXXXXX						XXXXXXXXXX									
010	[1]						XXXXXXXXXX									
011	XXXXXX						XXXXXXXXXX									
100	0	0	0	0	01111					1	0	0	1	1	0	[1]
101	1	00		1	00000					000			1	100		
110	010			0	0	011			00		0	[1]	0111			

[1] Undefined zone should always be programmed with 0.

7.8.2 Side band select

The image reject mixer can be programmed to either reject the image frequency at the LO upper frequency or at the LO lower frequency. If SBS = 0, frequency LO-IF is rejected; if SBS = 1, frequency LO+IF is rejected. It enables the user to have the RxLO in or out of ISM band and use the same IC in both handset and base.

7.8.3 Volume control

Software volume control on the earpiece amplifier is done with integrated switch feedback resistances.

Table 9. Software volume control

VCTRL1	VCTRL0	Select	Feedback resistance	Earpiece amplifier gain
0	0	0	14 kΩ	0 dB
0	1	1	24 kΩ	4.7 dB
1	0	2	41 kΩ	9.3 dB
1	1	3	70.2 kΩ	14 dB

Hardware volume control on the earpiece amplifier is done by switching externally the earpiece feedback resistance. Volume control is programmed to 3 (R_{int} = 70.2 kΩ). An example is given in Table 10.

Table 10. Hardware volume control example

Select	Feedback resistance	Earpiece amplifier gain
0	15 kΩ	−1.0 dB
1	33 kΩ	4.1 dB
2	100 kΩ	9.4 dB
3	open	14 dB

7.8.4 Second Filter Select (SFS)

Depending on the features of the IF filters used, the user might not need to use the second IF filter. In that case, bit SFS must be set to 0. When the second IF filter is used, SFS = 1. IF filters having 4.5 dB insertion loss are recommended.

Table 11. SFS

SFS value	Status
0	second IF filter unselect
1	second IF filter select

7.8.5 Data phase shifter

The SBS bit is used to invert the phase of the data. Depending on the SBS bit value and the protocol chosen, the data might be inverted between the base and handset data transmission. To correct the data polarity, the DATA Phase bit is set. When DATA Phase = 0, the inverter is bypassed; when DATA Phase = 1, the inverter is used.

7.8.6 PLL center frequency

This programming allows calibration of the center frequency of the VCO within the FM PLL to align the frequency as close as possible to the nominal 10.7 MHz frequency.

Table 12. VCO center frequency calibration

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Select	Center frequency shift (MHz)
0	0	0	0	0	0	+3.0
0	0	0	0	1	1	+2.8
0	0	0	1	0	2	+2.6
0	0	0	1	1	3	+2.4
0	0	1	0	0	4	+2.2
0	0	1	0	1	5	+2.0
0	0	1	1	0	6	+1.8
0	0	1	1	1	7	+1.6
0	1	0	0	0	8	+1.4
0	1	0	0	1	9	+1.2
0	1	0	1	0	10	+1.0
0	1	0	1	1	11	+0.8
0	1	1	0	0	12	+0.6
0	1	1	0	1	13	+0.4
0	1	1	1	0	14	+0.2
0	1	1	1	1	15	0
1	0	0	0	0	16	–0.2
1	0	0	0	1	17	–0.4
1	0	0	1	0	18	–0.6
1	0	0	1	1	19	–0.8
1	0	1	0	0	20	–1.0
1	0	1	0	1	21	–1.2
1	0	1	1	0	22	–1.4
1	0	1	1	1	23	–1.6
1	1	0	0	0	24	–1.8
1	1	0	0	1	25	–2.0
1	1	0	1	0	26	–2.2
1	1	0	1	1	27	–2.4
1	1	1	0	0	28	–2.6
1	1	1	0	1	29	–2.8
1	1	1	1	0	30	–3.0
1	1	1	1	1	31	–3.2

7.8.7 TX and TX gain programming registers

The TX and RX audio signal paths each have a programmable gain block. If a TX or RX voltage gain other than the nominal power-up default is desired, it can be programmed through the microcontroller interface. The gain blocks can be used during final test of the radio to electronically adjust for gain tolerances in the radio system. The RX and TX gain have steps of 0.5 dB covering a dynamic of –7.5 dB to +8 dB. At the earpiece output, the RX gain steps are multiplied by 2 due to the expander slope. The volume control feature for the earpiece amplifier allows for compensation of gain tolerances from –15 dB to +16 dB. Volume control is preferably done on the earpiece amplifier (see Section 7.8.3 “Volume control”).

Table 13. TX and RX gain

Gain control					Gain control	RX gain (dB)	EARO (dB)	TX gain (dB)
Bit 4	Bit 3	Bit 2	Bit 1	Bit 0				
0	0	0	0	0	0	–7.5	–15.0	–7.5
0	0	0	0	1	1	–7.0	–14.0	–7.0
0	0	0	1	0	2	–6.5	–13.0	–6.5
0	0	0	1	1	3	–6.0	–12.0	–6.0
0	0	1	0	0	4	–5.5	–11.0	–5.5
0	0	1	0	1	5	–5.0	–10.0	–5.0
0	0	1	1	0	6	–4.5	–9.0	–4.5
0	0	1	1	1	7	–4.0	–8.0	–4.0
0	1	0	0	0	8	–3.5	–7.0	–3.5
0	1	0	0	1	9	–3.0	–6.0	–3.0
0	1	0	1	0	10	–2.5	–5.0	–2.5
0	1	0	1	1	11	–2.0	–4.0	–2.0
0	1	1	0	0	12	–1.5	–3.0	–1.5
0	1	1	0	1	13	–1.0	–2.0	–1.0
0	1	1	1	0	14	–0.5	–1.0	–0.5
0	1	1	1	1	15	0	0	0
1	0	0	0	0	16	+0.5	+1.0	+0.5
1	0	0	0	1	17	+1.0	+2.0	+1.0
1	0	0	1	0	18	+1.5	+3.0	+1.5
1	0	0	1	1	19	+2.0	+4.0	+2.0
1	0	1	0	0	20	+2.5	+5.0	+2.5
1	0	1	0	1	21	+3.0	+6.0	+3.0
1	0	1	1	0	22	+3.5	+7.0	+3.5
1	0	1	1	1	23	+4.0	+8.0	+4.0
1	1	0	0	0	24	+4.5	+9.0	+4.5
1	1	0	0	1	25	+5.0	+10.0	+5.0
1	1	0	1	0	26	+5.5	+11.0	+5.5
1	1	0	1	1	27	+6.0	+12.0	+6.0
1	1	1	0	0	28	+6.5	+13.0	+6.5

Table 13. TX and RX gain *...continued*

Gain control					Gain control	RX gain (dB)	EARO (dB)	TX gain (dB)
Bit 4	Bit 3	Bit 2	Bit 1	Bit 0				
1	1	1	0	1	29	+7.0	+14.0	+7.0
1	1	1	1	0	30	+7.5	+15.0	+7.5
1	1	1	1	1	31	+8.0	+16.0	+8.0

7.8.8 Register content description

Table 14. Register content description

Data register	Bit	Description
ALC disable	1	automatic level control disable
	0	normal operation
Hard Limiter enable	1	hard limiter enable
	0	hard limiter disable
RX mute	1	RX channel muted
	0	normal operation
TX mute	1	TX channel muted
	0	normal operation
VREG enable	1	VREG enable
	0	VREG disable and tied to V_{CC} (in Inactive mode)
Earpiece enable	1	earpiece enable (can be used in RX mode for specific feature)
	0	earpiece disable

7.8.9 Voltage doubler

Minimum supply voltage for the IC is 2.9 V, which limits the voltage swing on both charge pumps to approximately 2.3 V. Using the voltage doubler or external high supply voltage on VCCCP pin, the increased voltage range enhances the tuning range of the VCOs varicaps. When Doubler = 1, the voltage doubler is active; when Doubler = 0, it is disabled. To save current in Inactive mode, the voltage doubler clock is the same as CLKO clock (can be programmed to XTAL / 128); in other mode, voltage doubler clock is XTALI divided by two.

7.8.10 Demodulator filter

An internal programmable filter limits the demodulator bandwidth. The –3 dB cut-off frequency of 7 kHz is selected with Demod Filter = 0 (default setting). With Demod Filter = 1, the –3 dB bandwidth is 100 kHz. The wider bandwidth provides a solution for audio and subaudio digital applications.

7.8.11 Active mode bits description

Table 15. Active mode bits description

Bit 1	Bit 0	Description
0	X	Inactive mode
1	0	RX mode
1	1	Active mode

[1] See details in Table 4 "Activated blocks".

7.8.12 Carrier detect threshold programming

When the Battery Detect active register = 0, the carrier detector is enabled and the signal CDout is routed to the output pin CDLBD. If RSSI is above the programmed RSSI level, CDLBD = 0, if not CDLBD = 1. The carrier detect gives an indication if a carrier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification section. If a different carrier detect threshold value is desired, it can be programmed through the microcontroller interface. To scale the carrier detect range, connect an external resistor from the RSSI pin to ground. CD control = (10011) which corresponds to RSSI = 0.86 V_{DC} (typical).

Table 16. Carrier detect

CD Bit 4	CD Bit 3	CD Bit 2	CD Bit 1	CD Bit 0	CD Control	RSSI voltage threshold detect (V)
0	0	0	0	0	0	0.1
0	0	0	0	1	1	0.14
0	0	0	1	0	2	0.18
0	0	0	1	1	3	0.22
0	0	1	0	0	4	0.26
0	0	1	0	1	5	0.3
0	0	1	1	0	6	0.34
0	0	1	1	1	7	0.38
0	1	0	0	0	8	0.42
0	1	0	0	1	9	0.46
0	1	0	1	0	10	0.5
0	1	0	1	1	11	0.54
0	1	1	0	0	12	0.58
0	1	1	0	1	13	0.62
0	1	1	1	0	14	0.66
0	1	1	1	1	15	0.7
1	0	0	0	0	16	0.74
1	0	0	0	1	17	0.78
1	0	0	1	0	18	0.82
1	0	0	1	1	19	0.86
1	0	1	0	0	20	0.9
1	0	1	0	1	21	0.94
1	0	1	1	0	22	0.98
1	0	1	1	1	23	1.02
1	1	0	0	0	24	1.06
1	1	0	0	1	25	1.1
1	1	0	1	0	26	1.14
1	1	0	1	1	27	1.18
1	1	1	0	0	28	1.22
1	1	1	0	1	29	1.26
1	1	1	1	0	30	1.3
1	1	1	1	1	31	1.34

7.8.13 Low battery detect

When the Battery Detect active register = 1, the low battery detect is enabled and the signal BDout is routed to the output pin CDLBD. If V_{CC} is below the LBD level programmed, CDLBD = 0, if not CDLBD = V_{CC}. The power-up default value is '110'.

Table 17. Low battery detect

Low battery detect			Select	Nominal low battery detect voltage (V)
Bit 2	Bit 1	Bit 0		
0	0	0	0	3.5
0	0	1	1	3.4
0	1	0	2	3.3
0	1	1	3	3.2
1	0	0	4	3.1
1	0	1	5	3.0
1	1	0	6	2.9
1	1	1	7	2.8

7.8.14 Clock output drive

Depending on the microcontroller clock frequency and clock capacitive load, the CLKO Drive can be programmed to optimize current consumption. CLKO Drive = 0 is designed for 10 MHz, 10 pF, and CLKO Drive = 1 for 10 MHz, 5 pF (or 5 MHz, 10 pF). The clock output level is $1.5V_{(p\text{-}p)}$. The CLKO output is AC-coupled with the XTALI pin of the microcontroller. External resonator from the microcontroller is then removed.

7.8.15 Clock output divider

The Clock Out signal is derived from the crystal oscillator and is used to drive a microcontroller (see Section 7.8.14). The crystal signal is divided down with a programmable divider value. To supply the clock to the microcontroller and save current in the handset, an external low power resonator may be used and the clock output disable (000) as well as the crystal oscillator (Xtal Active = 0). In power saving mode, divider ratio is programmed down to 128 to reduce the microcontroller power consumption.

Table 18. Clock output divider

Bit 2	Bit 1	Bit 0	Select	Clock divider ratio
0	0	0	1	output disable
0	0	1	2	2
0	1	0	3	2.5
0	1	1	4	4
1	0	0	5	1
1	1	1	6	128

7.8.16 Crystal HIGH

In Inactive mode, the crystal oscillator is a major contributor in the full current consumption. For a XTAL High = 0 (XTAL LOW), the current mode is programmed to save current yielding a full current consumption in Inactive mode at 230 μA (see details in Section 7.1.3 "Control bits in power saving modes"). When XTAL High = 1, the crystal oscillator current is increased by 100 μA.

7.8.17 Xtal tuning capacitors

An on-chip crystal reference tuning is provided to compensate for frequency spread over process and temperature. External capacitor on XTALI pin is chosen around 3 pF lower than on XTALO pin. Internally, a programmable capacitance is in parallel with the XTALI pin. Tuning capacitance values are in the range of 0 pF to 4.5 pF, as described in Table 19.

Table 19. Xtal tuning capacitors

Bit 3	Bit 2	Bit 1	Bit 0	Select	Capacitance (pF)
0	0	0	0	0	0.2
0	0	0	1	1	0.5
0	0	1	0	2	0.8
0	0	1	1	3	1.1
0	1	0	0	4	1.4
0	1	0	1	5	1.7
0	1	1	0	6	2.0
0	1	1	1	7	2.3
1	0	0	0	8	2.6
1	0	0	1	9	2.9
1	0	1	0	10	3.2
1	0	1	1	11	3.5
1	1	0	0	12	3.8
1	1	0	1	13	4.1
1	1	1	0	14	4.4
1	1	1	1	15	4.7

7.8.18 Expander noise level control

Depending on the application noise floor specification, a noise level control can be applied. At 00, it is disabled. At 11, it is forced to its maximum.

7.8.19 Power amplifier output level

The power amplifier uses 2 bits to modify the output power. PA is disabled for PA active = 0. A 300 Ω to 50 Ω matching (duplexer) is implemented with a parallel inductor and series C network. Output power for 50 Ω termination is specified in Table 20. To get the power at the antenna, the duplexer insertion loss should be subtracted. At maximum power, the DC current consumption is increased by 3 mA over the minimum power current consumption.

Table 20. Power amplifier output

PA active	PA bit 1	PA bit 0	Select	PA output power (dBm)	Second harmonic (dBm)	Third harmonic (dBm)	Fourth harmonic (dBm)
0	X	X	-	PA inactive	-	-	-
1	0	0	0	1	–17	–27	–34
1	0	1	1	1.9	–19	–29	–34
1	1	0	2	2.5	–23	–33	–36
1	1	1	3	3.0	–26	–36	–40

7.8.20 PLLs' charge pump current

Performance of the PLLs can be improved by increasing charge pump current. When Rx or Tx charge pump current bit is set to 0, current is 400 μA. When bit is set to 1, current is 800 μA. Rx and Tx charge pump currents are programmed independently.

7.8.21 Voltage reference adjustment

An internal 1.5 V band gap voltage reference provides the voltage reference for the low battery detect circuits, the VREG voltage regulator, the VB reference and all internal analog references. In Inactive mode, the adjustment is disabled.

Table 21. Voltage reference adjust

Voltage reference adjust			Select	Nominal voltage reference
Bit 2	Bit 1	Bit 0		
0	0	0	0	–7 %
0	0	1	1	–5 %
0	1	0	2	–3 %
0	1	1	3	–1 %
1	0	0	4	+1 %
1	0	1	5	+3 %
1	1	0	6	+5 %
1	1	1	7	+7 %

7.8.22 Test mode

Test mode bits are only used for test in production and application tuning. Those bits have to be set to 0 for normal operation. Out of lock of synthesizers Rx or Tx can be indirectly monitored on the CDLBD pin: the width of the 'glitch' gives a direct measure of the phase error on the PLL Rx and/or PLL Tx. To tune the external Rx and Tx VCOs inductors, a defined divided ratio has to be programmed on the dividers and then, the image of the VCO frequency can be read on the CDLBD pin. It can also be used to check the dividers ratio: force a frequency on VCOs or crystal pins and read the programmed frequency on CDLBD. Before the CDLBD pin, there is a divide-by-2, then all frequencies are divided by 2. When charge pumps are in 3-state, VCOs can be measured in stand alone.

Table 22. Test mode

Test bit 2	Test bit 1	Test bit 0	Select
0	0	0	normal operation
0	0	1	UP XOR DOWN RX
0	1	0	UP XOR DOWN TX
0	1	1	UP XOR DOWN RX or TX
1	0	0	reference divider output divided by 2
1	0	1	prescaler and main divider RX divided by 2
1	1	0	prescaler and main divider TX divided by 2
1	1	1	double synthesizers charge pump are in 3-state

8. Limiting values

Table 23. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+6.0	V
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature	operating	–20	+80	°C

9. Thermal characteristics

Table 24. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; SA58646BD	68	K/W

10. Characteristics

Table 25. Characteristics

V_{CC} = 3.3 V; T_{amb} = 25 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{CC}	supply voltage			2.9	3.3	5.5	V
T_{amb}	ambient temperature	operating		–20	-	+80	°C
FM receiver part (RXRF)							
Low noise amplifier and image reject mixer (f_o = 903 MHz)							
R_{iRX}	RF input resistance (real part of the parallel input impedance)	balanced; indicative		-	110	-	Ω
C_{iRX}	RF input capacitance (imaginary part of the parallel input impedance)	balanced; indicative		-	0.7	-	pF
f_{iRX}	RF input frequency			902	903	928	MHz
RL_{iRX}	return loss on match RF input		[1]	10	-	-	dB
G_{CPRX}	conversion power gain	balun input to MIXO pin matched to 330 Ω		-	22	-	dB
$CP1_{RX}$	1 dB input compression point		[1]	-	–23	-	dBm
$IP3_{RX}$	3rd order intercept point			-	–13	-	dBm
NF_{RX}	overall RF front end noise figure (does not include the IF section)			-	4	5	dB
IR	image frequency rejection	in band of interest		26	45	-	dB
R_{LRX}	IF resistive output load	on MIXO pin; indicative		-	330	-	W
C_{LRX}	IF capacitive output load	on MIXO pin; indicative		-	-	3	pF

Table 25. Characteristics
V_{CC} = 3.3 V; T_{amb} = 25 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
IF amplifier section (f_o = 10.7 MHz)							
G_{IFAMP1}	first IF amplifier voltage/power gain; measured at amplifier output	330 Ω matched input and output; SFS = 1		-	22.5	-	dB
NF_{IFAMP1}	first IF amplifier noise figure	330 Ω matched input and output		-	7	-	dB
G_{IFAMP2}	second IF amplifier voltage/power gain; measured at amplifier output	330 Ω matched input and output; SFS = 1		-	25	-	dB
NF_{IFAMP2}	second IF amplifier noise figure	330 Ω matched input and output		-	14	-	dB
G_{IFAMP}	IF amplifier gain	330 Ω matched input and output; SFS = 0		-	43	-	dB
NF_{IFAMP}	IF amplifier noise figure			-	7.5	-	dB
PLL demodulator (f_o = 10.7 MHz; f_{dev} = ±25 kHz; f_{mod} = 1 kHz)							
$\Delta f_{VCO}/\Delta V$	VCO gain	after calibration		-	760	-	KHz/V
f_{VCO}	VCO center frequency (free running)	open loop; all conditions		7.0	10.7	15.0	MHz
$N_{step(VCO)}$	VCO frequency adjust: number of steps			-	32	-	steps
BW_{demod}	demodulator −3 dB bandwidth	Demod Filter = 0; Loop filter: 4.7 kΩ; 1.8 nF; 150 pF		-	7	-	kHz
		Demod Filter = 1; Loop filter: 15 kΩ; 150 pF; 12 pF		-	100	-	kHz
F_{DEVmax}	maximum frequency deviation					±75	kHz
$f_{VCO(st)}$	VCO center frequency step			-	200	-	kHz
$R_{L(PLL)}$	demodulator external load on pin DETO			5	-	-	kΩ
$V_{o(PLL)(rms)}$	output voltage on pin DETO; Tx Mode	$R_{L(PLL)}$ = 10 kΩ; amplifier gain = 10	[2]	-	100	350	mVrms
$V_{o(PLL)(DC)}$	DC output voltage on pin DETO; adjust with microcontroller			1.2	1.4	1.6	V
FM receiver system characteristics: f_o = 903 MHz; f_{dev} = ±25 kHz; f_{mod} = 1 kHz; Demod Filter = 0; $R_{L(EARO)}$ = 150 Ω in series with 10 μF(all with CCITT filter)							
S_{RFI}	sensitivity (BW = 100 kHz)	at antenna with 3 dB duplexer insertion loss					
	input level for 12 dB sinad	Rx mode		-	−115	-	dBm
		Tx mode; PA = 10; V(EARO) = 200 mVrms; minimum Tx-Rx duplexer isolation: 35 dB		-	−113.5	-	dBm
S/N_{FM}	signal to noise ratio	$V_{i(RFin)}$ = −80 dBm and −40 dBm; Txmode; PA = 10; CLKO OFF; V(EARO) = 200 mVrms		40	45	-	dB

Table 25. Characteristics

V_{CC} = 3.3 V; T_{amb} = 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD_{FM}	total harmonic distortion at f_{dev} = ±60 kHz (without CCITT filter)	$V_{i(RFin)}$ = −80 dBm and −40 dBm Tx mode; PA = 10; CLKO OFF; V(EARO) = 500 mVrms	-	0.6	2	%
RSSI/Carrier Detect: V_B = 1.5 V						
RSSI	output current dynamic range		-	68	-	dB
V_{OH}	HIGH-level output voltage	CDLBDout output; $V_{i(LIM)}$ = 0 mV (RMS); CD = (10011);	$0.9V_{CC}$	-	-	V
V_{OL}	LOW-level output voltage	CDLBDout output; $V_{i(LIM)}$ = 0.1 V (RMS); CD = (10011);	-	-	$0.1V_{CC}$	V
R_{int}	internal resistance value	between RSSI and V_{CC}	-	175	-	kΩ
V_{det}	voltage detection range		0.05	-	1.6	V
$V_{det(st)}$	voltage detection step		-	40	-	mV
V_{hys}	hysteresis voltage		-	45	-	mV
$N_{step(CD)}$	carrier sense threshold: number of steps	programmable through microcontroller	-	32	-	steps
Data comparator						
$V_{i(DATC)}$	comparator input signal		100	-	-	mV_{p-p}
$V_{hys(DATC)}$	hysteresis		25	40	75	mV
$V_{th(DATC)}$	threshold voltage on pin DATAI		-	V_{CC} −0.9	-	V
$Z_{i(DATC)}$	input impedance at DATAI		150	240	-	kΩ
V_{OH}	HIGH-level output voltage	$V_{i(DATAI)}$ = V_{CC} −1.4 V	$0.9V_{CC}$	-	-	V
V_{OL}	LOW-level output voltage	$V_{i(DATAI)}$ = V_{CC} −0.4 V	-	-	$0.1V_{CC}$	V
I_{OH}	output sink current on DATAO pin	$V_{i(DATAI)}$ = V_{CC} −0.4 V $V_{o(DATAO)}$ = 0.1 V_{CC}	-	50	-	µA
The transmit part						
Summator amplifier						
$V_{o(SUM)}$	summator output voltage on pin MODO		-	94	240	mV_{p-p}
$R_{f(SUM)}$	summator external feedback resistor	between MODI and MODO	10	-	-	kΩ
$V_{bias(SUM)}$	DC voltage at pin MODI		-	2.2	-	V
Tx voltage control oscillator and power amplifier						
$f_{VCO(TX)}$	oscillator free running frequency	[1]	-	910	-	MHz
$Q_{L(VCO(TX))}$	external inductor quality factor at 902 MHz to 928 MHz	L = 3.9 nH	30	-	-	
$\Delta f_{VCO(TX)}/\Delta V_{TXLF}$	VCO gain	V_{TXLF} = 0.5 V	-	50	-	MHz/V
		V_{TXLF} = 1.5 V	-	25	-	MHz/V
$\Delta f_{VCO(TX)}/\Delta V_{mod}$	VCO modulation gain	V_{MODO} = 2.2 V	-	530	-	kHz/V

Table 25. Characteristics
V_{CC} = 3.3 V; T_{amb} = 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{VCO(TX)}$	VCO TX + PA phase noise	output power 0 dBm; Tx → Rx duplexer isolation = 35 dB; carrier = 925.6 MHz; L_{ext} = 3.9 nH (for both base and handset); loop filter: C1 = 470 nF; R2 = 1.8 kΩ; C2 = 4.7 μF (see application note)				
		f_{offset} = 20 MHz	–139	–150	-	dBc/Hz
		f_{offset} = 10 kHz	-	–85	-	dBc/Hz
		f_{offset} = 1 kHz	-	–60	-	dBc/Hz
V_{PA}	PA output power range	R = 50 Ω; L_p = 22 nH; C_s = 1.6 pF	-	2	-	dB
$N_{step(PA)}$	PA output voltage number of steps		-	4	-	steps
$V_{o(PA)}$	PA output power (11)	remove duplexer insertion loss to get power on antenna; R = 50 Ω; L_p = 22 nH; C_s = 1.6 pF	-	+3	-	dBm
Transmit system						
THD_{TX}	total harmonic distortion after demodulation	V_{MODO} for demodulated f_{dev} = ± 60 kHz; measured with CCITT filter	-	1	2	%
$ISO_{(RX-TX)}$	RxVCO spurious emission on PA output versus output power	[1]	-	–45	-	dBc
The synthesizer						
Crystal oscillator; external capacitor on XTALO = 8.2 pF; XTALI = 5.6 pF (indicative)						
f_{XTAL}	reference input frequency from crystal		4	10.24	20	MHz
C_{XTALI}	input capacitance	indicative; XTALCap = 8	-	4	-	pF
C_{XTALO}	input capacitance	indicative	-	1.5	-	pF
C_{TUNE}	crystal tuning capacitance range	on XTALI pin	-	4.5	-	pF
$C_{step(TUNE)}$	number of capacitor tuning steps		-	16	-	steps
Reference and clock divider						
R_{RDR}	reference divider ratio		8	-	1023	
R_{CDR}	clock divider ratio	5 steps (2, 2.5, 4, 1, 128)	1	-	128	
$C_{L(CLK)}$	clock output load capacitance	external	-	-	20	pF
$V_{O(CLK)}$	clock output voltage swing on pin CLKO	CLKO drive = 1; 10 MHz, 5 pF (or 5 MHz, 10 pF)	-	1.5	-	V_{p-p}
		CLKO drive = 0; 10 MHz, 10 pF	-	1.5	-	V_{p-p}

Table 25. Characteristics
V_{CC} = 3.3 V; T_{amb} = 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sw(f1-f2)}$	switching time from one frequency f1 to frequency f2		-	2 / f2	-	s
RF Tx and Rx prescaler and main dividers						
f_{RF}	RF input frequency		902	903	928	MHz
R_{PDR}	prescaler ratio		64	-	127	
R_{MDR}	main divider ratio		8	-	1023	
Charge pump current						
I_{RxCP}	Rx charge pump sink or source current	RxCPI = 0	-	400	-	µA
		RxCPI = 1	-	800	-	µA
I_{TxCP}	Tx charge pump sink or source current	TxCPI = 0	-	400	-	µA
		TxCPI = 1	-	800	-	µA
Rx voltage control oscillator						
f_{VCO}	oscillator free-running frequency	[1]	-	910	-	MHz
$Q_{L(VCO(RX))}$	external inductor quality factor at 920 MHz	L = 3.9 nH	30	-	-	
$\Delta f_{VCO(RX)}/\Delta V_{RXLF}$	VCO gain	L_{ext} = 4.7 nH at 890 MHz, 3.9 nH at 935 MHz				
		V_{TXLF} = 0.5 V	-	55	-	MHz/V
		V_{TXLF} = 1.5 V	-	30	-	MHz/V
$N_{VCO(RX)}$	VCO RX phase noise	indicative: cannot be directly measured carrier = 892.3 MHz; L_{ext} = 4.7 nH (3.9 nH for 935 MHz operation) loop filter: C1 = 3.9 nF; R2 = 6.8 kΩ; C2 = 47 nF (see application note)				
		f_{offset} = 1 kHz	-	−58	-	dBc/Hz
		f_{offset} = 10 kHz	-	−82	-	dBc/Hz
		f_{offset} = 100 kHz	-	−102	-	dBc/Hz
Voltage doubler						
$V_{CC(CP)}$	charge pump supply voltage	doubler = 1; V_{CC} = 3 V	-	5.2	-	V
The RX baseband						
RX audio path (RX gain adjust/RX mute/expander) (see Figure 6): VB = 1.5 V; f = 1 kHz; RX gain set for 0 dB gain at −20 dBV on RXAI; Volume Control = 1 (+4.7 dB) with 560 pF between EARI, EARO; (all measured with a CCITT filter except THDs), RL(EARO) = 150 Ω in series with 10 µF						
ΔG_{ARX}	RX gain adjustment range	programmable through microcontroller interface				
		on Rx Gain amplifier	−7.5	-	+8	dB
		measured on EARO	−15	-	+16	dB
$N_{step(ARX)}$	RX gain adjust steps	programmable through microcontroller interface	-	32	-	steps
$\Delta G_{v(m)}$	RX mute	$V_{i(RXAI)}$ = −20 dBV	-	−70	−60	dB

Table 25. Characteristics
V_{CC} = 3.3 V; T_{amb} = 25 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
G_{EXP}	expander gain level	$V_{i(RXAI)}$ = –20 dBV		–1	0	+1	dB
ΔG_{EXP}	expander gain change	referenced to $V_{i(RXAI)}$ = –20 dBV with Rx baseband audio noise tuning	[4]				
		$V_{i(RXAI)}$ = –30 dBV		–24	–20	–18	dB
		$V_{i(RXAI)}$ = –35 dBV		–37	–30	–26	dB
		$V_{i(RXAI)}$ = –45 dBV		-	–47	–45	dB
$V_{i(RXAI)}$	maximum input voltage	THD < 4 %		-	–13	-	dBV
$V_{o(EXPout)}$	maximum output voltage; indicative	THD < 4 %		-	–7	-	dBV
N_{ARX}	audio path noise	BW = 300 Hz to 3.4 kHz		-	–83	-	dBVp
$Z_{i(RXAI)}$	input impedance	in TX mode	[2]	-	15	-	kΩ
		in RX mode	[2]	100	-	-	kΩ
$t_{att(EXP)}$	expander attack time	E_{cap} = 0.47 μF		-	2.0	-	ms
$t_{rel(EXP)}$	expander release time	E_{cap} = 0.47 μF		-	5.0	-	ms
$\alpha_{ct(EXPout)}$	compressor to expander crosstalk attenuation	$V_{(RXAI)}$ = 0 V(RMS); from CMPI to EARO $V_{i(CMPI)}$ = –20 dBV		-	80	-	dB
$V_{O(EARO)(max)}$	maximum output swing value	THD < 4 %		-	2.2	-	V_{p-p}
$R_{L(EARout)}$	earpiece output impedance to keep amplifier stability	in series with 10 μF		-	150	100 k	Ω
V_{Ctrl}	volume control	no external resistor or capacitor used					
		VCtrl = 00		–1	0	+1	dB
		VCtrl = 01		3.7	4.7	5.7	dB
		VCtrl = 10		8.3	9.3	10.3	dB
		VCtrl = 11		13	14	15	dB
$V_{Ctrl(dyn)}$	volume control dynamic range			13	14	15	dB
THD_{ARX}	total harmonic distortion	$V_{i(RXAI)}$ = –20 dBV		-	0.2	2	%
The TX baseband							
Microphone amplifier (VB = 1.5 V; f = 1 kHz)							
$V_{o(MICO)}$	maximum output voltage	R_L = 10 kΩ; THD < 0.2 %		–12	-	-	dBV
ΔG_V	voltage gain range			0	-	34	dB
TX audio path (compressor/ALC/TX mute/TX gain adjust (see Figure 7): VB = 1.5 V; f = 1 kHz; TX Gain set for +10 dB gain at –30 dBV on $V_{i(CMPI)}$							
G_{COMP}	compressor gain level	ALC off, HLim = 0; $V_{i(CMPI)}$ = –30 dBV		+9	+10	+11	dB
ΔG_{COMP}	compressor gain level difference	referenced to $V_{i(CMPI)}$ = –30 dBV					
		$V_{i(CMPI)}$ = –10 dBV		+8	+10	+12	dB
		$V_{i(CMPI)}$ = –50 dBV		–14	–10	–8	dB

Table 25. Characteristics
V_{CC} = 3.3 V; T_{amb} = 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_{COMP(max)}$	maximum compressor gain	$V_{i(CMPI)}$ = –70 dBV	-	23	-	dB
V_{HLIM}	output voltage Hard limiter	ALC off; HLim = 1; $V_{i(CMPI)}$ = –4 dBV	-	1.26	-	V_{p-p}
$V_{o(TXO)}$	maximum output voltage range ALC on	$V_{i(CMPI)}$ = –12 dBV	-	–12.5	-	dBV
		$V_{i(CMPI)}$ = –10 dBV	-	–12.3	-	dBV
		$V_{i(CMPI)}$ = –2.5 dBV	-	–11.5	-	dBV
THD_{COMP}	total harmonic distortion ALC off	$V_{i(CMPI)}$ = –10 dBV	-	0.5	2	%
$Z_{i(CMPI)}$	input impedance		-	15	-	kΩ
$t_{att(COMP)}$	compressor attack time	C_{cap} = 0.47 μF	-	4.0	-	ms
$t_{rel(COMP)}$	compressor release time	C_{cap} = 0.47 μF	-	8.0	-	ms
$\alpha_{ct(COMP)}$	expander to compressor crosstalk attenuation	$V_{(CMPI)}$ = 0 Vrms; from RXAI to TXO; $V_{i(RXAI)}$ = –10 dBV	-	65	-	dB
$\Delta G_{v(m)}$	TX mute ALC off	$V_{i(CMPI)}$ = –10 dBV	-	–70	–60	dB
ΔG_{ATX}	TX gain adjustment range	programmable through microcontroller interface	–7.5	-	+8	dB
$N_{step(ATX)}$	TX gain adjustment steps	programmable through microcontroller interface	-	32	-	steps
$Z_{o(TXO)}$	output impedance at pin TXO		-	500	-	Ω
Other features						
PLL voltage regulator						
V_{REG}	regulated output voltage level	VregEn = 0	-	V_{CC}	-	V
		VregEn = 1				
		before V_{ref} adjustment or in Inactive mode	2.5	2.7	2.9	V
		after V_{ref} adjustment	2.65	2.7	2.75	V
I_O	output current	C_{VREG} = 1 μF	-	-	3	mA
Low battery detect; LBD Active = HIGH						
LBD_{steps}	number of detection steps		-	8	-	steps
LBD_{level}	detection voltage range		2.8	-	3.5	V
V_{hys}	comparator hysteresis	$(V_{HIGH} - V_{LOW}) \times (VB / V_{THRES})$	-	18	-	mV
$\Delta V_{CC} / V_{CC}$	battery detect accuracy	after VRef adjust; BD = (010)	-	0.5	5	%

Table 25. Characteristics

V_{CC} = 3.3 V; T_{amb} = 25 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Microcontroller serial interface							
Digital pins in DC							
V_{IL}	LOW-level input voltage	pins DATA, CLK, EN		-	-	0.5	V
V_{IH}	HIGH-level input voltage	pins DATA, CLK, EN		V_{REG} / 1.5	-	V_{CC}	V
I_{IL}	LOW-level input current	pins DATA, CLK, EN; V_{IL} = 0.3 V		−5	-	-	mA
I_{IH}	HIGH-level input current	pins DATA, CLK, EN; V_{IH} = V_{REG} −0.3 V		-	-	5	mA
I_{OL}	LOW-level output current	pin CDLBD		20	-	-	mA
V_{OL}	LOW-level output voltage	pin CDLBD; R_L = 470 kΩ		-	-	0.1V_{CC}	V
V_{OH}	HIGH-level output voltage	pin CDLBD; R_L = 470 kΩ		0.9V_{CC}	-	-	V
C_i	input capacitance	pins DATA, CLK, EN		-	-	8	pF
C_o	output capacitance	pins RXPD, TXPD		-	-	8	pF
Digital pins timing (see Figure 11)							
$t_{su(CLK-EN)}$	CLK to EN setup time	50 % of signals		50	-	-	ns
$t_{su(DATA-CLK)}$	DATA to CLK setup time	50 % of signals		50	-	-	ns
$t_{h(EN-CLK)}$	EN to CLK hold time	50 % of signals		50	-	-	ns
f_{clk}	clock frequency			-	-	3	MHz
$t_{r(i)}$	input rise time	pins DATA, CLK, EN; 10 % to 90 %		-	-	50	ns
$t_{f(i)}$	input fall time	pins DATA, CLK, EN; 10 % to 90 %		-	-	50	ns
$t_{h(EN)end}$	EN hold time at end of word			100	-	-	ns
$t_{W(i)(EN)}$	input pulse width at pin EN		[3]	1 / f_{comp}	-	-	ns
$t_{start(MCU)}$	microcontroller interface start-up time	90 % of V_{REFPLL} to DATA, CLK, EN		-	-	200	µs

[1] That spec will be measured and guaranteed only on the Philips SA58646 board.

[2] RXAI level will be higher in RX mode than in TX mode.

[3] The minimum pulse width should be equal to the period of the comparison frequency. The synthesizer checks the internal EN signal not to happen during a comparison phase to avoid any phase error jump. Then this time can be reduced to 100 ns for words that do not influence the synthesizer (word 1, word 2, word 3).

[4] With expander output noise level control tuned for −65 dBV (max) and gain tolerance (max) of −4 dB at −35 dBV. With a larger gain tolerance at −35 dBV, the typical output noise can be reduced by 10 dB. See application note.

11. Application information

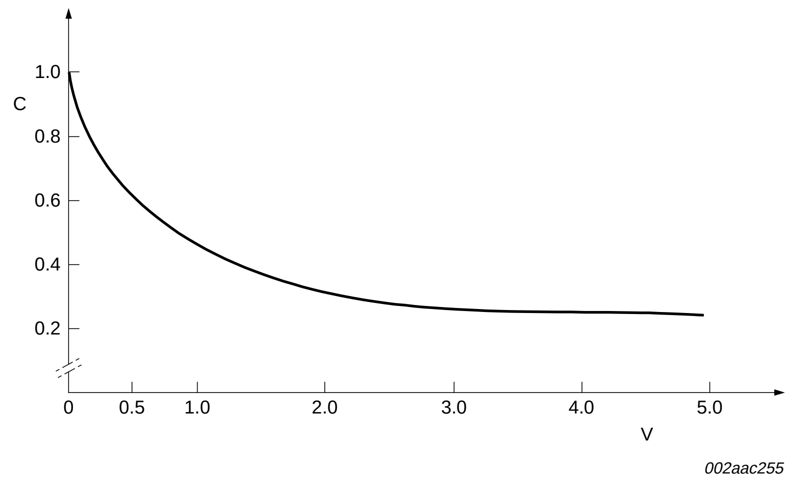
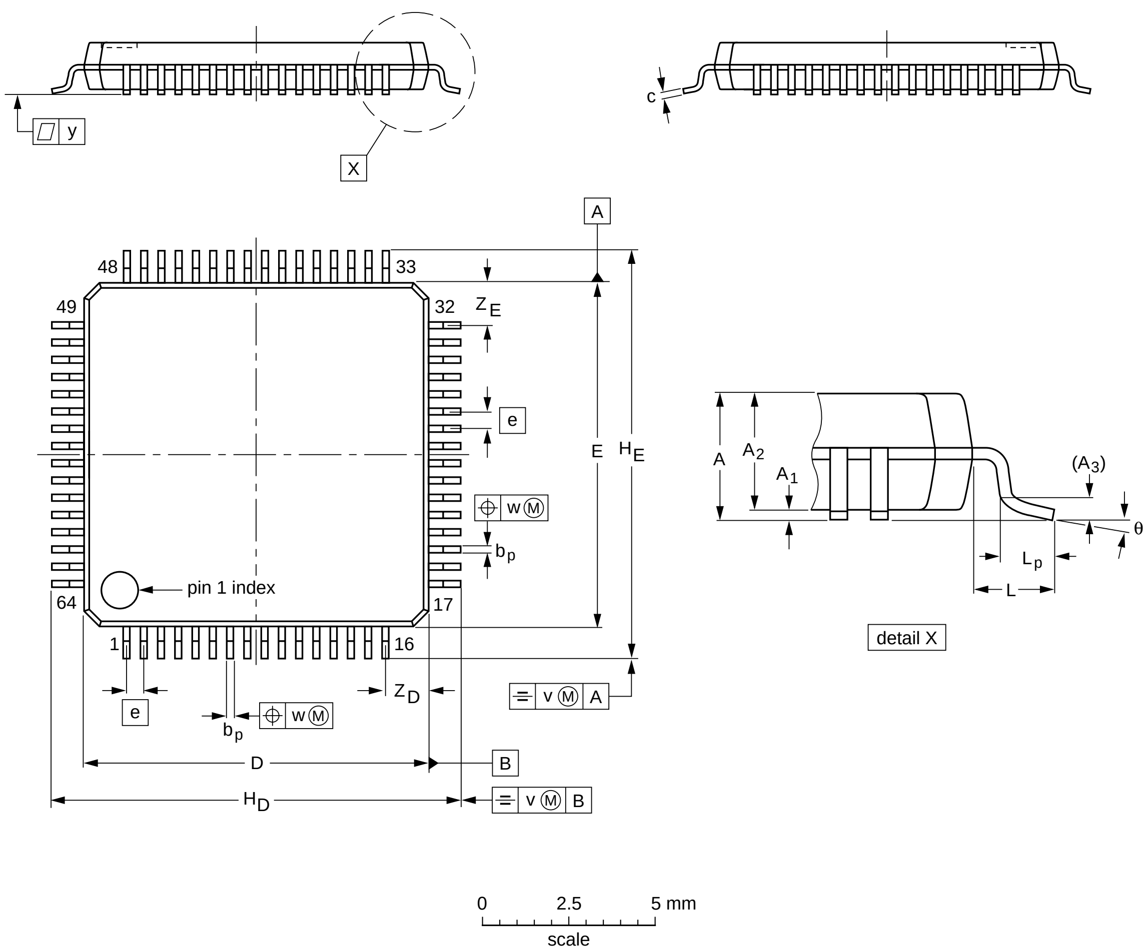


Fig 12. Varicap behavior

12. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 13. Package outline <package version> (<package name>)

13. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

14. Soldering

14.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 26. SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 °C + 0/–5 °C	225 °C + 0/–5 °C
≥ 2.5 mm	225 °C + 0/–5 °C	225 °C + 0/–5 °C

Table 27. Pb-free process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 350 to 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 28. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Abbreviations

Table 29. Abbreviations

Acronym	Description
ALC	Automative Loop Control
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
FM	Frequency Modulation
IF	Intermediate Frequency
ISM	Industrial, Medical and Scientific
LNA	Low Noise Amplifier
PA	Power Amplifier
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
VCO	Voltage Controlled Oscillator

16. Revision history

Table 30. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SA58646_1.05	20060714	Objective data sheet	-	SA58646_1.04
SA58646_1.04	20060425	Objective data sheet	-	SA58646_1.03
SA58646_1.03	20060424	Objective data sheet	-	SA58646_1.02
SA58646_1.02	20060424	Objective data sheet	-	SA58646_1.01
SA58646_1.01	20060329	Objective data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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19. Contents

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